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EXAMINER	
CONNOLLY, MARK A	

ART UNIT	PAPER NUMBER
2185	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/595,198	Applicant(s) FLEISCHMANN ET AL.	
	Examiner Mark Connolly	Art Unit 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14 and 15* is/are allowed.

6)☒ Claim(s) *1,3,4,7,10-13 and 16-19* is/are rejected.

7)☒ Claim(s) *2,5,6,8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-19 have been presented for examination.

2. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear if "loading *said context* in said internal memory" is referring to CPU or Northbridge context. For examining purposes, the said context is interpreted as Northbridge context.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 16 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Byrd US Pat No 4763333.

6. Referring to claim 16, Byrd teaches the invention substantially including:

   a. a processor [13 fig. 3].

   b. a first memory accessible by said processor [14 fig. 3].

c. a second memory assessable only to said processor, wherein power to said second memory is controlled separately from power to said processor and to said first memory, wherein power is maintained to said second memory when power is removed from said processor, said second memory for maintaining internal context of said processor when power is removed from said processor [Abstract, col. 2 line 65 - col. 3 line 12 and 20 fig. 3]. Because the processor loads data from the second memory into the first memory rather than a memory controller, it is interpreted that the second memory is only accessible by the processor.

7. Referring to claim 17, Byrd teaches that the second memory is external to the processor [20 fig. 3].

Claim Rejections - 35 USC § 103

8. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

9. Claims 1, 3, 4 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicants Admitted Prior Art [AAPA] in view of Sasscer US Pat No 4523206.

10. Referring to claim 1, the AAPA teaches the invention substantially including:

a. determining if a prescribed period of inactivity has been attained, and, in response to an affirmative determination [page 2 lines 3-5].

i. preserving the internal context of a processor against loss due to removal of electrical power from the processor [page 3 lines 12-19].

ii. removing all electrical power from the processor, whereby the processor is powered down, notwithstanding continued supply of electrical power to the computer [page 2 lines 6-14].

iii. restoring electrical power to the processor and restoring the preserved internal context to the processor when processing is to resume [page 2 line 22 – page 3 line 19].

The AAPA does not explicitly teach preserving the internal context in a private memory accessible only by the processor and powered independently of the processor.

Sasscer explicitly teaches that the context of a processor can be preserved by powering the cache memory separately from the rest of the processor [col. 5 lines 54-60]. The cache memory is interpreted as a memory accessible only to the processor. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the AAPA to maintain power to the processor cache because it would allow the AAPA-Sasscer system to wake from a sleep state faster. The AAPA explicitly teaches that as CPU context is sent to system memory and then to hard disk in order to be preserved, the wake time for the system increases. It should be apparent that it would have been an obvious design choice to preserve the CPU context by maintaining power to just the cache while shutting down the rest of the processor because although it would not provide as much power savings as the AAPA system alone would provide, but it would still provide some power savings in that some power could be removed from the processor but would allow the processor to wake up much faster because the context would not have to be loaded back into the CPU from an external memory when the system wakes.

11. Referring to claim 3, Sasscer teaches powering the cache separately from the processor [col. 5 lines 54-60].

12. Referring to claim 4, the AAPA teaches initializing the processor and determining if the power was removed due to a power on reset or an STR [page 4 lines 13-16]. The AAPA also teaches that if it has been determined that the power removal was due to an STR to access and install the preserved processor context [page 4 lines 16-21].

13. Referring to claim 12, this is rejected on the same basis as set forth hereinabove.

14. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Sasscer as applied to claims 1, 3, 4 and 12 above, and further in view of Song et al[1] [Song] U.S. Pat. No. 5991531.

15. Referring to claim 13, the AAPA-Sasscer system as described above does not explicitly teach the computer comprising a host computer for dynamically translating and executing instructions of a target application designed for processing by a target computer containing an instruction set different from the instruction set of the host computer. In summary, the AAPA-Sasscer system does not teach translating and executing instructions, which are designed to run on a separate computer, to run on a host computer. Song does explicitly teach translating and executing instructions, which are designed to run on a separate computer, to run on a host computer [col. 1 lines 45-52, col. 3 lines 26-29 and 35-39]. The vector processor architecture that permits emulation of double-width operations is interpreted as the host computer. The 64-byte operations are interpreted as the instruction set designed for processing by a separate target

[1] As cited in the previous office action

computer and which is also different from the instruction set of the host computer. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the AAPA-Sasscer system to allow the emulation and process of instructions that are designed to run on a separate computer because it would allow the AAPA-Sasscer system to support the longer data width operations, which are more common in newer processors, while still maintaining a reduced chip size, cost and code length as taught by Song [col. 2 lines 41-43].

16. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai[2] US Pat No 6266776 in view of AAPA.

17. Referring to claim 7, Sakai teaches the invention substantially including:

a. a CPU for processing instructions of an application, the CPU including internal registers. It is well known that CPU's comprise internal registers.

b. a first and second memory [col. 1 lines 49-51]. The non-volatile storage is interpreted to be the first memory and the system memory is interpreted to be the second memory. In addition, memory is interpreted as something that stores information.

c. a power supply for supplying power separately to the CPU and the first and second memory [col. 1 lines 39-41 and lines 49-51]. It can be seen that in the S2 state, the CPU is powered down separately from the first and second memories. It isn't until later in the S4 state that the first and second memories are powered off. In addition, it is well known in the art that a computer system will put a hard disk into a standby or sleep state, is independent of the power state of the rest of the system, which essentially shuts

[2] As cited in the previous office action

down the motor in the hard disk in order to conserve power. The hard disk is interpreted as a non-volatile memory which was interpreted as a first memory. Therefore it can be seen that a CPU, first and second memory would each reside in separate power domains.

d. a power supply including a battery [col. 1 lines 13-14].

e. a first and second power circuit means for distributing electrical power to the CPU and the first and second memories respectfully. It is inherent that Sakai comprises a first and second power means to distribute power to the CPU and first and second memories respectfully

f. an on-off switch for closing power from said battery to each of the first and second power circuit means whereby the first and second power circuit means is enabled to deliver power. This on-off switch is interpreted as a main power on/off switch of a computer system.

g. a first program routine means for detecting inactivity of application instruction processing of the CPU for a period of time [col. 6 lines 56-58].

Sakai does not explicitly teach:

h. a second program routine means for saving the entire internal context of the CPU in the second memory and for producing an STR signature in response to a positive detection of inactivity by the first program routine means

i. a third program means for terminating distribution of power by the first power circuit means following completion of the second program routine means, whereby power is removed from the CPU while the internal context of the CPU is preserved in the second memory.

The AAPA teaches:

j. a second program routine means for saving the entire internal context of the CPU in the second memory and for producing an STR signature in response to a positive detection of inactivity by the first program routine means [col. 4 lines 1-4 and 13-16]. The DRAM memory and system memory of Sakai are interpreted to be the same. In addition, it is obvious that the AAPA would produce a signature because it provides a way for the operating system to determine if an STR occurred so that it can resume from STR. Because the signature alerts the system that a Resume from STR should occur, the signature inherently indicates that the second memory contains CPU context. The CPU context is interpreted as information.

k. a third program means for terminating distribution of power by the first power circuit means following completion of the second program routine means, whereby power is removed from the CPU while the internal context of the CPU is preserved in the second memory [page 3 lines 23-25 and page 4 lines 1-4].

It would have been obvious to one of ordinary skill in the art to modify Sakai to include the teachings of AAPA because the AAPA teaches that it is desirable to preserve the processor context when entering an STR sleep mode so that the context is available for later use when restoring the processor from the sleep mode.

18. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai and AAPA as applied to claim 7 above, and further in view of Tanenbaum[3].

[3] As cited in the previous office action

19. Referring to claim 10, this is rejected on the same basis as set forth in the rejection for claim 7 with the exception that the Sakai-AAPA system does not explicitly teach a code morphing program means defining a virtual X86 processing system. The Sakai –AAPA system does not explicitly teach a virtual X86 processing system including a virtual X86 CPU and virtual Northbridge chip where the instructions of the X86 application program may be processed in the processing system. In summary, the Sakai – AAPA system does not explicitly teach software versions of the CPU and Northbridge chip to execute the instructions of the X86 application program.

Tanenbaum teaches "Hardware and software are logically equivalent" [page 11 line 11]. Tanenbaum then goes further and teaches that hardware can be simulated in software [page 11 line 13]. Therefore it would have been obvious to one of ordinary skill in the art to modify the Sakai –AAPA system to include a virtual CPU and Northbridge because both can perform the same operations. Furthermore, an artisan would also be motivated to create a virtual CPU and a virtual Northbridge because it would reduce the size and cost of a system in comparison to a system where the same CPU and Northbridge was realized in hardware.

20. Referring to claim 11, this is rejected on the same basis as set forth hereinabove.

21. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byrd as applied to claims 16 and 17 above, and further in view of Sasscer US Pat No 4523206.

22. Referring to claim 18, Byrd does not teach that the processor context can be preserved internal to the processor. Sasscer explicitly teaches that the cache of a processor can be powered independently [col. 5 lines 54-60]. It would have been obvious to one of ordinary skill in the art

at the time of the invention to modify the Byrd system to power the cache independently because then the processor context could be preserved without having to transfer the context to an external memory. The cache now being interpreted as a second memory

23. Referring to claim 19, the Byrd-Sasscer system still includes an aux memory external to the processor [20 fig. 3 of Byrd] which stores the state of the OS and memory 14 as described above. Therefore, the Byrd-Sasscer system teaches a third memory external to the processor.

Allowable Subject Matter

24. Claims 14-15 are allowed.

25. Claims 2, 5, 6, 8 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. US Pat No 5036455 to Atwood. This teaches saving a processor state in a battery backed memory.

b. US Pat No 5617572 to Pearce et al. This teaches that hard disks can be put into a sleep or standby mode independently from the rest of the system.

c. US Pat No 5765001 to Clark et al. This teaches that processor context is stored in a special memory location

d. US Pat No 5898880 to Ryu. This teaches that a hard disk can sleep independently from the rest of the system.

e. US Pat No 5935259 to Anderson. This teaches battery powering the processor in order to preserve its context.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark Connolly whose telephone number is (703) 305-7849. The examiner can normally be reached on M-F 8AM-5PM (except every first Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Mark Connolly
Examiner
Art Unit 2185

mc

November 12, 2003

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100